What is claimed is:

1. A memory cell, comprising:

an access transistor having a floating node, the floating node to store a charge indicative of a memory state of the memory cell; and

a diode exhibiting Negative Differential Resistance (NDR) behavior connected between the floating node and a diode reference potential line, the diode including an anode, a cathode and an intrinsic region between the anode and the cathode, the intrinsic region of the diode to assist with stabilizing the memory state of the memory cell.

2. The memory cell of clam 1, wherein the cathode of the diode is connected to the floating node of the access transistor.

3. The memory cell of claim 1, wherein the diode is a gate-controlled diode.

4. The memory cell of claim 1, wherein the access transistor is formed in a bulk semiconductor structure.

5. The memory cell of claim 1, wherein the access transistor is formed in a semiconductor-on-insulator structure.

6. A memory cell, comprising:

an access transistor having a first diffusion region connected to a bit line, and a second diffusion region, the second diffusion region to store a charge indicative of a memory state of the memory cell;

a Negative Differential Resistance (NDR) diode connected between the second diffusion region and a diode reference potential line, the diode including: an

anode; a cathode; an intrinsic region between the anode and cathode to assist with stabilizing the memory state of the memory cell; and a diode gate operatively positioned with respect to the intrinsic region to enhance switching performance between memory states.

7. A memory cell, comprising:

an n-channel access transistor on a bulk semiconductor substrate, the n-channel access transistor having a first n-type diffusion region connected to a bit line and a second n-type diffusion region, the second n-type diffusion region to store a charge indicative of a memory state of the memory cell; and

a Negative Differential Resistance (NDR) n/i/p diode having an n-type anode connected to a diode reference potential line, a p-type cathode in contact with the second n-type diffusion region, and an intrinsic region between the anode and the cathode to assist with stabilizing the memory state of the memory cell.

8. A memory cell, comprising:

a p-channel access transistor on a bulk semiconductor substrate, the p-channel access transistor having a first p-type diffusion region connected to a bit line and a second p-type diffusion region, the second p-type diffusion region to store a charge indicative of a memory state of the memory cell; and

a Negative Differential Resistance (NDR) n/i/p diode having an n-type anode connected to a diode reference potential line, a p-type cathode formed with the second n-type diffusion region, and an intrinsic region between the anode and the cathode to assist with stabilizing the memory state of the memory cell.

9. A memory cell, comprising:

an n-channel access transistor on a bulk semiconductor substrate, the p-channel access transistor having a first n-type diffusion region connected to a bit line

and a second n-type diffusion region, the second n-type diffusion region to store a charge indicative of a memory state of the memory cell; and

a Negative Differential Resistance (NDR) p/i/n diode having a p-type anode connected to a diode reference potential line, an n-type cathode formed with the second n-type diffusion region, and an intrinsic region between the anode and the cathode to assist with stabilizing the memory state of the memory cell.

10. A memory cell, comprising:

a p-channel access transistor on a bulk semiconductor substrate, the p-channel access transistor having a first p-type diffusion region connected to a bit line and a second p-type diffusion region, the second p-type diffusion region to store a charge indicative of a memory state of the memory cell; and

a Negative Differential Resistance (NDR) p/i/n diode having a p-type anode connected to a diode reference potential line, an n-type cathode in contact with the second p-type diffusion region, and an intrinsic region between the anode and the cathode to assist with stabilizing the memory state of the memory cell.

11. A memory cell, comprising:

an access transistor on a bulk semiconductor substrate, the access transistor having a first diffusion region connected to a bit line and a second diffusion region, the second diffusion region to store a charge indicative of a memory state of the memory cell; and

a Negative Differential Resistance (NDR) diode connected between the second diffusion region of the access transistor and a diode reference potential line, the diode having an anode, a cathode, and an intrinsic region between the anode and the cathode to assist with stabilizing the memory state of the memory cell, the diode being laterally oriented over the access transistor.

12. A memory cell, comprising:

an access transistor on a bulk semiconductor substrate, the access transistor having a first diffusion region connected to a bit line and a second diffusion region, the second diffusion region to store a charge indicative of a memory state of the memory cell; and

a Negative Differential Resistance (NDR) diode connected between the second diffusion region of the access transistor and a diode reference potential line, the diode having an anode, a cathode, and an intrinsic region between the anode and the cathode to assist with stabilizing the memory state of the memory cell, the diode being vertically oriented over the access transistor.

13. A memory cell, comprising:

an n-channel access transistor on a semiconductor-on-insulator substrate, the n-channel access transistor having a floating body and a first n-type diffusion region connected to a bit line and a second n-type diffusion region, the second n-type diffusion region to store a charge indicative of a memory state of the memory cell; and

a Negative Differential Resistance (NDR) n/i/p diode having an n-type anode connected to a diode reference potential line, a p-type cathode in contact with the second n-type diffusion region, and an intrinsic region between the anode and the cathode to assist with stabilizing the memory state of the memory cell,

wherein intentionally-generated charges in the floating body of the access transistor enhance diode switching.

14. A memory cell, comprising:

a p-channel access transistor on a semiconductor-on-insulator substrate, the p-channel access transistor having a floating body and a first p-type diffusion region connected to a bit line and a second p-type diffusion region, the second p-type

diffusion region to store a charge indicative of a memory state of the memory cell; and

a Negative Differential Resistance (NDR) n/i/p diode having an n-type anode connected to a diode reference potential line, a p-type cathode formed with the second n-type diffusion region, and an intrinsic region between the anode and the cathode to assist with stabilizing the memory state of the memory cell,

wherein intentionally-generated charges in the floating body of the access transistor enhance diode switching.

15. A memory cell, comprising:

an n-channel access transistor on a semiconductor-on-insulator substrate, the p-channel access transistor having a floating body and a first n-type diffusion region connected to a bit line and a second n-type diffusion region, the second n-type diffusion region to store a charge indicative of a memory state of the memory cell; and

a Negative Differential Resistance (NDR) p/i/n diode having a p-type anode connected to a diode reference potential line, an n-type cathode formed with the second n-type diffusion region, and an intrinsic region between the anode and the cathode to assist with stabilizing the memory state of the memory cell,

wherein intentionally-generated charges in the floating body of the access transistor enhance diode switching.

16. A memory cell, comprising:

a p-channel access transistor on a semiconductor-on-insulator substrate, the p-channel access transistor having a floating body and a first p-type diffusion region connected to a bit line and a second p-type diffusion region, the second p-type diffusion region to store a charge indicative of a memory state of the memory cell; and

a Negative Differential Resistance (NDR) p/i/n diode having a p-type anode connected to a diode reference potential line, an n-type cathode in contact with the second p-type diffusion region, and an intrinsic region between the anode and the cathode to assist with stabilizing the memory state of the memory cell,

wherein intentionally-generated charges in the floating body of the access transistor enhance diode switching.

17. A memory cell, comprising:

an access transistor on a semiconductor-on-insulator substrate, the access transistor having a floating body and a first diffusion region connected to a bit line and a second diffusion region, the second diffusion region to store a charge indicative of a memory state of the memory cell; and

a Negative Differential Resistance (NDR) diode connected between the second diffusion region of the access transistor and a diode reference potential line, the diode having an anode, a cathode, and an intrinsic region between the anode and the cathode to assist with stabilizing the memory state of the memory cell, the diode being laterally oriented in the floating body of the access transistor,

wherein intentionally-generated charges in the floating body of the access transistor enhance diode switching.

18. A memory cell, comprising:

an access transistor on a semiconductor-on-insulator substrate, the access transistor having a floating body and a first diffusion region connected to a bit line and a second diffusion region, the second diffusion region to store a charge indicative of a memory state of the memory cell; and

a Negative Differential Resistance (NDR) diode connected between the second diffusion region of the access transistor and a diode reference potential line, the diode having an anode, a cathode, and an intrinsic region between the anode and

the cathode to assist with stabilizing the memory state of the memory cell, the diode being laterally oriented over the access transistor,

wherein intentionally-generated charges in the floating body of the access transistor enhance diode switching.

19. A memory cell, comprising:

an access transistor on a semiconductor-on-insulator substrate, the access transistor having a floating body and a first diffusion region connected to a bit line and a second diffusion region, the second diffusion region to store a charge indicative of a memory state of the memory cell; and

a Negative Differential Resistance (NDR) diode connected between the second diffusion region of the access transistor and a diode reference potential line, the diode having an anode, a cathode, and an intrinsic region between the anode and the cathode to assist with stabilizing the memory state of the memory cell, the diode being vertically oriented over the access transistor,

wherein intentionally-generated charges in the floating body of the access transistor enhance diode switching.

20. A memory cell, comprising:

an access transistor, including:

a body region;

a first diffusion region electrically connected to a bit line;

a second diffusion region separated from the first diffusion region by a channel area in the body region;

a gate separated from the channel area by a gate insulator, the gate electrically connected to a word line;

a Negative Differential Resistance (NDR) diode, including an anode, a cathode, and an intrinsic region between the anode and the cathode, the diode being connected between the second diffusion region and a diode reference potential line,

wherein the memory cell is operative to store and sense a charge in the second diffusion region that is representative of a memory state.

21. The memory cell of claim 20, wherein the access transistor includes an n-channel transistor.

22. The memory cell of claim 20, wherein the access transistor includes a p-channel transistor.

23. The memory cell of claim 20, wherein the diode includes a p/i/n diode having a p-type anode, an n-type cathode, and an intrinsic region between the anode and cathode.

24. The memory cell of claim 23, wherein the p/i/n diode includes a p+/i/n+ diode having a p+ anode an n+ cathode, and an intrinsic region between the anode and cathode.

25. The memory cell of claim 20, wherein the diode includes an n/i/p diode having an n-type anode, a p-type cathode, and an intrinsic region between the anode and cathode.

26. The memory cell of claim 25, wherein the n/i/p diode includes an n+/i/p diode having an n+ anode, a p cathode, and an intrinsic region between the anode and cathode.

27. The memory cell of claim 20, wherein the diode includes a laterally-oriented diode.

28. The memory cell of claim 20, wherein the diode includes a vertically-oriented diode.

29. The memory cell of claim 20, wherein the intrinsic region has a predetermined geometry to assist with stabilizing the memory state of the memory cell.

30. The memory cell of claim 20, wherein the diode includes a gate-controlled diode to enhance switching performance and reduce standby power.

31. The memory cell of claim 20, wherein the access transistor is on a semiconductor-on-insulator substrate.

32. The memory cell of claim 20, wherein the access transistor is on a bulk semiconductor substrate.

33. A memory cell, comprising:

an access transistor formed in a bulk semiconductor structure, the access transistor including a first diffusion region separated from a second diffusion region by a channel region, and further including a gate separated from the channel region by a gate insulator, wherein the first diffusion region is connected to a bit line and the gate is connected to a first word line; and

a gate-controlled Negative Differential Resistance (NDR) diode connected between a reference potential line and the second diffusion region, the diode including an anode, a cathode, an intrinsic region positioned between the anode and

the cathode, and a diode gate operably positioned with respect to the intrinsic region, the diode gate being connected to a second word line.

34. The memory cell of claim 33, wherein the diode is formed such that the intrinsic region has a desired geometry to assist with stabilizing the memory state of the memory cell

35. The memory cell of claim 33, wherein the gate-controlled diode includes a laterally-oriented diode positioned over the access transistor.

36. The memory cell of claim 35, wherein the lateral-orientated diode is formed using raised source/drain techniques and metal-induced-lateral crystallization techniques.

37. The memory cell of claim 33, wherein the gate-controlled diode includes a vertically-oriented diode.

38. The memory cell of claim 33, wherein:

the first and second diffusion regions of the access transistor include n-type dopants; and

the gate-controlled diode includes a p/i/n diode having a p-type anode connected to the reference potential line and an n-type cathode formed with the second diffusion region.

39. The memory cell of claim 33, wherein:

the first and second diffusion regions of the access transistor include n-type dopants; and

the gate-controlled diode includes an n/i/p diode having an n-type anode connected to the reference potential line and a p-type cathode in contact with the second diffusion region.

40. The memory cell of claim 33, wherein:

the first and second diffusion regions of the access transistor include p-type dopants; and

the gate-controlled diode includes a p/i/n diode having a p-type anode connected to the reference potential line and an n-type cathode in contact with the second diffusion region.

41. The memory cell of claim 33, wherein:

the first and second diffusion regions of the access transistor include n-type dopants; and

the gate-controlled diode includes an n/i/p diode having an n-type anode connected to the reference potential line and a p-type formed with the second diffusion region.

42. A memory cell, comprising:

an semiconductor-on-insulator (SOI) structure, including an SOI access transistor including a first diffusion region separated from a second diffusion region by a channel region, and further including a gate separated from the channel region by a gate insulator, wherein the first diffusion region is connected to a bit line and the gate is connected to a first word line; and

a Negative Differential Resistance (NDR) diode connected between the second diffusion region and a reference potential line, the diode including an anode, a cathode, and an intrinsic region between the anode and the cathode.

43. The memory cell of claim 42, wherein the diode is formed such that the intrinsic region has a desired geometry to store a charge indicative of a memory state.

44. The memory cell of claim 42, wherein the diode includes a gate-controlled diode having a diode gate operably positioned with respect to the intrinsic region, the diode gate being connected to a second word line.

45. The memory cell of claim 42, wherein the diode includes a lateral-oriented diode.

46. The memory cell of claim 45, wherein the lateral-oriented diode is positioned over the access transistor and is formed using raised source/drain techniques and metal-induced-lateral crystallization techniques.

47. The memory cell of claim 45, wherein the SOI access transistor and the lateral-oriented diode are formed in a semiconductor volume over a buried oxide (BOX) region.

48. The memory cell of claim 42, wherein the diode includes a vertical-oriented diode.

49. The memory cell of claim 48, wherein the vertical-oriented diode includes the second diffusion region of the access transistor.

50. The memory cell of claim 42, wherein:

the first and second diffusion regions of the access transistor include n-type dopants; and

the gate-controlled diode includes a p/i/n diode having a p-type anode connected to the reference potential line and an n-type cathode formed with the second diffusion region.

51. The memory cell of claim 42, wherein:

the first and second diffusion regions of the access transistor include n-type dopants; and

the gate-controlled diode includes an n/i/p diode having an n-type anode connected to the reference potential line and a p-type cathode in contact with the second diffusion region.

52. The memory cell of claim 42, wherein:

the first and second diffusion regions of the access transistor include p-type dopants; and

the gate-controlled diode includes a p/i/n diode having a p-type anode connected to the reference potential line and an n-type cathode in contact with the second diffusion region.

53. The memory cell of claim 42, wherein:

the first and second diffusion regions of the access transistor include n-type dopants; and

the gate-controlled diode includes an n/i/p diode having an n-type anode connected to the reference potential line and a p-type formed with the second diffusion region.

54. A memory cell, comprising:

an access transistor, the access transistor including a first diffusion region separated from a second diffusion region by a channel region, and further including

a gate separated from the channel region by a gate insulator, wherein the first diffusion region is connected to a bit line and the gate is connected to a first word line; and

a Negative Differential Resistance (NDR) p/i/n diode connected between a diode reference potential line and the second diffusion region, the p/i/n diode including a p-type anode, an n-type cathode, and an intrinsic region positioned between the anode and the cathode.

55. The memory cell of claim 54, wherein the p/i/n diode includes a p+/i/n+ diode include a p+ anode, an n+ cathode, and an intrinsic region positioned between the anode and the cathode.

56. The memory cell of claim 54, wherein the diode includes a gate-controlled diode having a diode gate operably positioned with respect to the intrinsic region, the diode gate being connected to a second word line.

57. The memory cell of claim 54, wherein the access transistor and the diode are on a semiconductor-on-insulator (SOI) substrate.

58. The memory cell of claim 54, wherein the access transistor and the diode are on a bulk semiconductor substrate.

59. The memory cell of claim 54, wherein the diode includes a laterally-oriented diode.

60. The memory cell of claim 54, wherein the diode includes a vertically-oriented diode.

61. The memory cell of claim 54, wherein the access transistor includes a p-channel transistor.

62. The memory cell of claim 54, wherein the access transistor includes an n-channel transistor.

63. A memory cell, comprising:

an access transistor, including a first diffusion region separated from a second diffusion region by a channel region, and further including a gate separated from the channel region by a gate insulator, wherein the first diffusion region is connected to a bit line and the gate is connected to a first word line; and

a Negative Differential Resistance (NDR) n/i/p diode connected between a diode reference potential line and the second diffusion region, the n/i/p including an n-type anode, a p-type cathode, and an intrinsic region positioned between the anode and the cathode.

64. The memory cell of claim 63, wherein the n/i/p diode includes an n+/i/p diode, including an n+ anode, a p cathode, and an intrinsic region positioned between the anode and the cathode.

65. The memory cell of claim 63, wherein the diode includes a gate-controlled diode having a diode gate operably positioned with respect to the intrinsic region, the diode gate being connected to a second word line.

66. The memory cell of claim 63, wherein the access transistor and the diode are on a semiconductor-on-insulator (SOI) substrate.

67. The memory cell of claim 63, wherein the access transistor and the diode are on a bulk semiconductor substrate.

68. The memory cell of claim 63, wherein the diode includes a laterally-oriented diode.

69. The memory cell of claim 63, wherein the diode includes a vertically-oriented diode.

70. The memory cell of claim 63, wherein the access transistor includes a p-channel transistor.

71. The memory cell of claim 63, wherein the access transistor includes an n-channel transistor.

72. A memory device, comprising:

a memory array, including a plurality of memory cells in rows and columns;

a number of word lines, each word line connected to a row of memory cells;

a number of bit lines, each bit line connected to a column of memory cells;

at least one reference line to provide a reference potential to the memory cells;

control circuitry, including word line select circuitry and bit line select circuitry to select a number of memory cells for writing and reading operations,

wherein each memory cell includes:

an access transistor, including a body region, a first diffusion region electrically connected to one of the bit lines, a second diffusion region separated from the first diffusion region by a channel area in the body region, and a gate separated from the

channel area by a gate insulator and electrically connected to one of the word lines; and

a Negative Differential Resistance (NDR) diode, including an anode, a cathode, and an intrinsic region between the anode and the cathode, the diode being connected between the second diffusion region and a diode reference line,

wherein the memory cell is adapted to store a charge in the second diffusion region of the access transistor to indicate a stable memory state.

73. The memory device of claim 72, wherein the diode includes a gate-controlled diode.

74. The memory device of claim 72, wherein each memory cell is on a bulk semiconductor substrate, and the diode includes a vertically-oriented diode.

75. The memory device of claim 72, wherein each memory cell is on a bulk semiconductor substrate, and the diode includes a laterally-oriented diode over the access transistor.

76. The memory device of claim 72, wherein each memory cell is on a semiconductor-on-insulator substrate such that the access transistor has a floating body, and the diode includes a vertically-oriented diode.

77. The memory device of claim 76, wherein the vertical-oriented diode is at least partially formed in the floating body of the access transistor.

78. The memory device of claim 72, wherein each memory cell is on a semiconductor-on-insulator substrate such that the access transistor has a floating body, and the diode includes a laterally-oriented diode formed in the floating body of the access transistor.

79. The memory device of claim 72, wherein each memory cell is on a semiconductor-on-insulator substrate, and the diode includes a laterally-oriented diode over the access transistor.

80. A method for operating a memory cell, comprising:

selectively switching a diode with an intrinsic region between a conducting "on" state and a non-conducting "off" state to represent a binary memory state, wherein the intrinsic region is between a cathode and an anode of the diode; and

sensing the binary memory state, including connecting a bit line to the diode and detecting a bit line potential change based on current flowing through the diode.

81. The method of claim 80, wherein selectively switching a diode includes pulsing a diode gate to enhance switching performance for write operations.

82. The method of claim 80, wherein selectively switching a diode includes generating a charge in a floating body of the access transistor to enhance switching performance for write operations.

83. The method of claim 80, wherein selectively switching a diode includes:

performing a write-one operation to store a first memory state, including forward biasing the diode to provide the conducting "on" state; and

performing a write-zero operation to store a second memory state, including reverse biasing the diode to provide the non-conducting "off" state.

84. A method for operating a memory cell, comprising:

performing a write-one operation, including actuating an access transistor to electrically connect a bit line to a floating node of the access transistor, and forward biasing a diode connected to the floating node of an access transistor such that a charge is stored on the floating node to hold the diode in a conducting "on" state;

performing a read-one operation, including actuating the access transistor to electrically connect the bit line to the floating node, and sensing a significant change in a bit line potential attributed to current flowing through the diode and the access transistor;

performing a write-zero operation, including actuating the access transistor to electrically connect the bit line to the floating node, reverse biasing the diode and holding the diode in a non-conducting "off" state; and

performing a read-zero operation, including actuating the access transistor to electrically connect the bit line to the floating node, and sensing that there is not a significant change to the bit line potential.

85. A method for forming a memory cell, comprising:

forming an access transistor with a floating node, the floating node to store a charge indicative of a memory state of the memory cell; and

forming a Negative Differential Resistance (NDR) diode connected between the floating node and a reference potential line, wherein forming a diode includes forming a diode with an intrinsic region between a cathode and an anode of the diode, the intrinsic region having a desired geometry to assist with stabilizing the memory state of the memory cell.

86. The method of claim 85, wherein forming a diode with an intrinsic region between a cathode and an anode of the diode includes forming a diode with an

intrinsic region between a p-type anode connected to the reference potential line and an n-type cathode connected to the floating node of the access transistor.

87. The method of claim 86, further comprising integrating the n-type cathode with an n-type diffusion region that forms the floating node of the access transistor.

88. The method of claim 86, further comprising forming the n-type cathode to interface with a p-type diffusion region that forms the floating node of the access transistor.

89. The method of claim 85, wherein forming a diode with an intrinsic region between a cathode and an anode of the diode includes forming a diode with an intrinsic region between an n-type anode connected to the reference potential line and a p-type cathode connected to the floating node of the access transistor.

90. The method of claim 89, further comprising integrating the p-type cathode with a p-type diffusion region that forms the floating node of the access transistor.

91. The method of claim 89, further comprising forming the p-type cathode to interface with an n-type diffusion region that forms the floating node of the access transistor.

92. The method of claim 85, wherein forming an access transistor with a floating node includes forming a p-channel access transistor.

93. The method of claim 85, wherein forming an access transistor with a floating node includes forming an n-channel access transistor.

94. The method of claim 85, wherein forming an access transistor with a floating node includes forming an access transistor in a bulk semiconductor substrate.

95. The method of claim 85, wherein forming an access transistor with a floating node includes forming an access transistor in a semiconductor-on-insulator (SOI) substrate.

96. The method of claim 85, wherein forming a diode connected between the floating node and a reference potential line includes forming a vertically-oriented diode.

97. The method of claim 96, wherein forming an access transistor with a floating node includes forming the access transistor in a semiconductor volume over a buried oxide region, and forming the vertically-oriented diode includes forming the diode in the semiconductor volume over the BOX region.

98. The method of claim 85, wherein forming a diode connected between the floating node and a reference potential line includes forming a laterally-oriented diode.

99. The method of claim 98, wherein forming an access transistor with a floating node includes forming the access transistor in a semiconductor volume over a buried oxide region, and forming the laterally-oriented diode includes forming the diode in the semiconductor volume over the BOX region.

100. The method of claim 98, wherein forming the laterally-oriented diode includes forming a raised floating node using a raised source-drain technology, and

forming a crystalline lateral structure in contact with the raised floating node using a metal-induced-lateral-crystallization process.